Y24KPA

PHASE CONTROL THYRISTOR

Features：

- **n** Center amplifying gate
- **n** Metal case with ceramic insulator
- **n** Low on-state and switching losses

Typical Applications

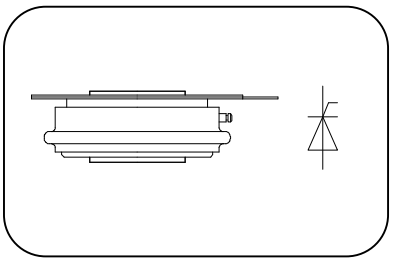
- **n** AC controllers
- **n** DC and AC motor control
- **n** Controlled rectifiers

$I_{T(AV)}$ **477A**

V_{DRM}/V_{RRM} **200~600V**

I_{TSM} **6.0 KA**

I^2t **180 10^3A^2S**



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled T_{hs}=55°C	125			477	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V	125	200		600	V
I_{DRM} I_{RRM}	Repetitive peak current	V_{DM}= V_{DRM} V_{RM}= V_{RRM}	125			16	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			6	KA
I^2t	I^2T for fusing coordination					180	A^2S*10^3
V_{TO}	Threshold voltage		125			0.83	V
r_T	On-state slop resistance					0.61	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1000A, F=5.0KN	125			1.44	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			300	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to 800A, Gate pulse t_r ≤0.5 μ s I_{GM}=1.5A Repetitive	125			100	A/μs
I_{rm}	Reverse recovery current	I_{TM}=500A,tp=1000μs, di/dt=-20A/μs, V_R =50V	125			100	A
t_{rr}	Reverse recovery time					12	μs
Q_{rr}	Recovery charge					600	μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	35		200	mA
V_{GT}	Gate trigger voltage			0.8		2.0	V
I_H	Holding current			20		150	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.25			V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At 180^0 sine, double side cooled Clamping force 5.0KN				0.095	°C /W
F_m	Mounting force			3.3		5.5	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				55		g
Outline	KT19aT						

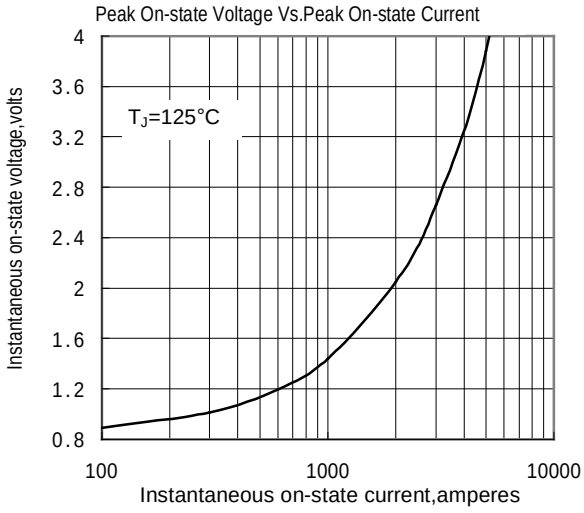


Fig.1

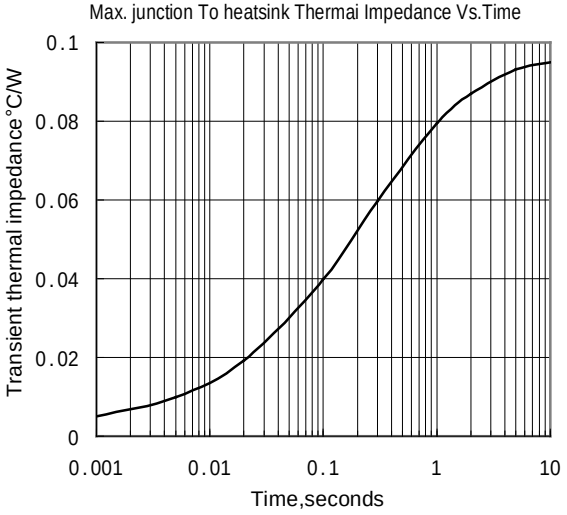


Fig.2

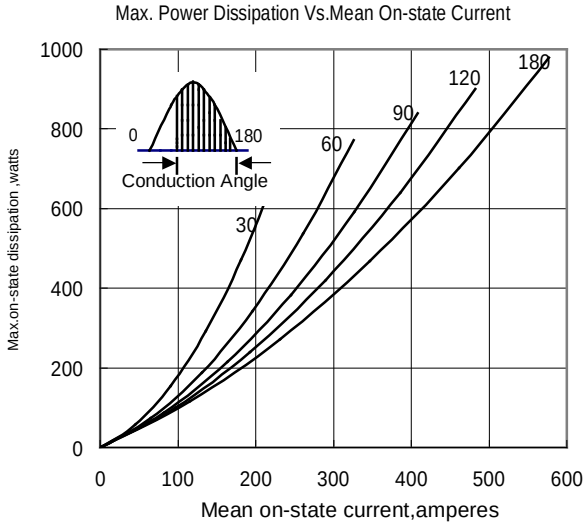


Fig.3

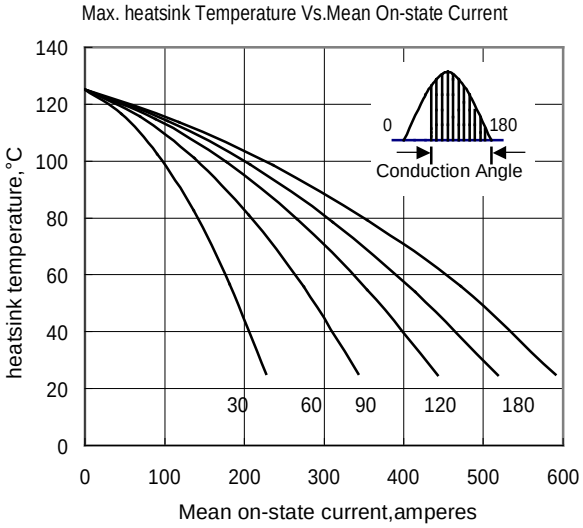


Fig.4

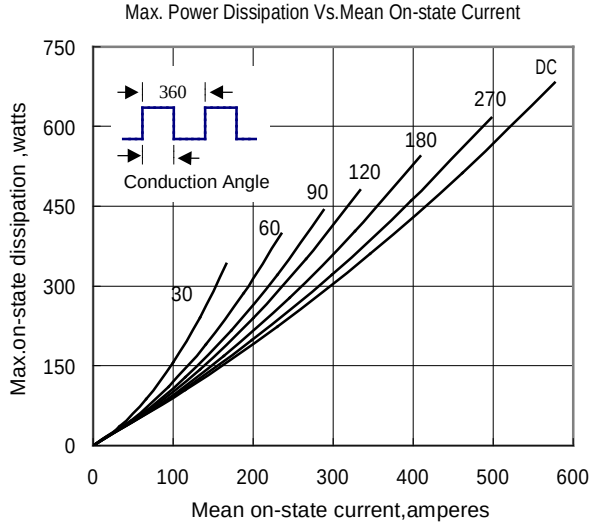


Fig.5

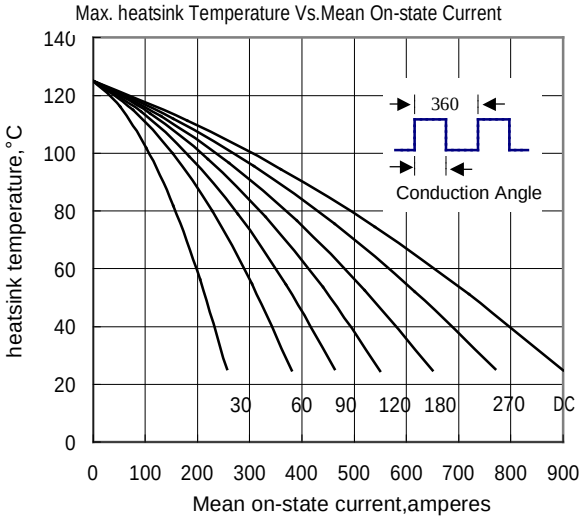


Fig.6

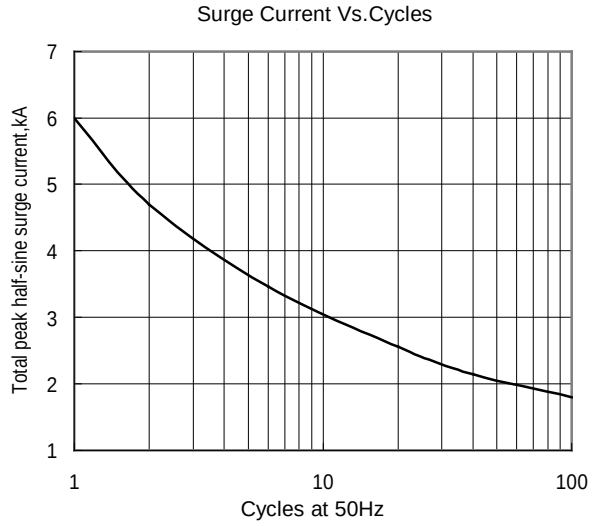


Fig.7

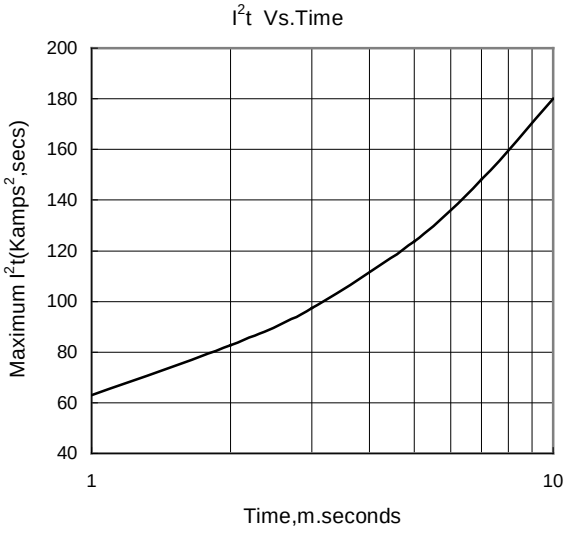


Fig.8

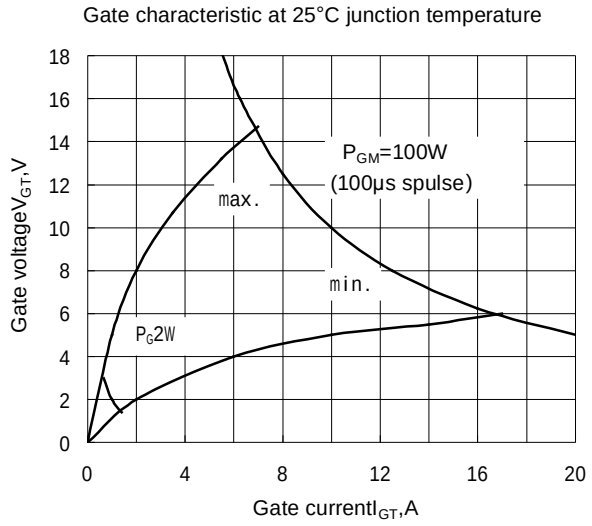


Fig.9

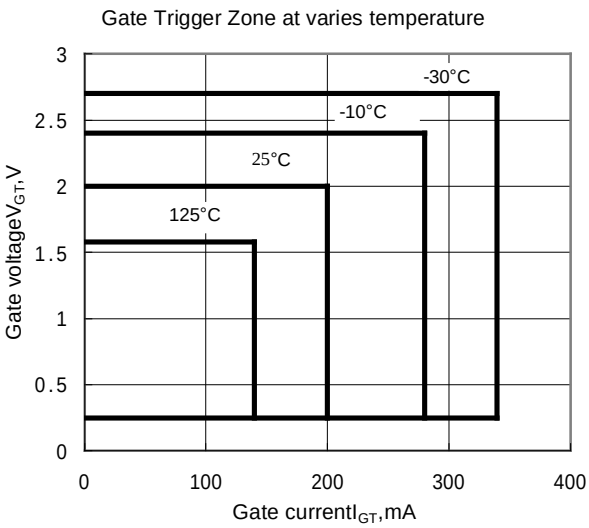


Fig.10

Outline: