

Y50KPH

PHASE CONTROL THYRISTOR

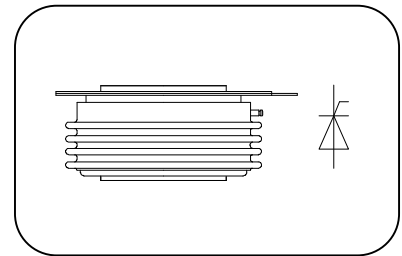
Features:

- n Center amplifying gate
- n Metal case with ceramic insulator
- n Low on-state and switching losses

Typical Applications

- n AC controllers
- n DC and AC motor control
- n Controlled rectifiers

$I_{T(AV)}$ **1293A**
 V_{DRM}/V_{RRM} **1900~3000V**
 I_{TSM} **15.5 KA**
 I^2t **1201 10³A²S**



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T _f (°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, T _{hs} =55°C	125			1293	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM} & V_{RRM} tp=10ms V_{DSM} & $V_{RSM}= V_{DRM}$ & V_{RRM} +100V	125	1900		3000	V
I_{DRM} I_{RRM}	Repetitive peak current	$V_{DM}= V_{DRM}$ $V_{RM}= V_{RRM}$	125			80	mA
I_{TSM}	Surge on-state current	10ms half sine wave	125			15.5	KA
I^2t	I ² T for fusing coordination	$V_R=0.6V_{RRM}$				1201	A ² s*10 ³
V_{TO}	Threshold voltage		125			1.11	V
r_T	On-state slop resistance					0.36	mW
V_{TM}	Peak on-state voltage	$I_{TM}=2400A$, F=24KN	125			1.97	V
dv/dt	Critical rate of rise of off-state voltage	$V_{DM}=0.67V_{DRM}$	125			500	V/μs
di/dt	Critical rate of rise of on-state current	$V_{DM}= 67\%V_{DRM}$ to2600A, Gate pulse t _r ≤0.5 μ s I _{GM} =1.5A Repetitive	125			150	A/μs
I_{rm}	Reverse recovery current		125			178	A
t_{rr}	Reverse recovery time	$I_{TM}=1300A$, tp=1000μs, di/dt=-20A/μs, $V_R=50V$				17.8	μs
Q_{rr}	Recovery charge					1588	μC
I_{GT}	Gate trigger current		25	40		300	mA
V_{GT}	Gate trigger voltage	$V_A=12V$, I _A =1A		0.8		3.0	V
I_H	Holding current			20		300	mA
V_{GD}	Non-trigger gate voltage	$V_{DM}=67\%V_{DRM}$	125	0.3			V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At 180° sine double side cooled Clamping force 24KN				0.024	°C /W
F_m	Mounting force			19		26	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				470		g
Outline	KT50cT						

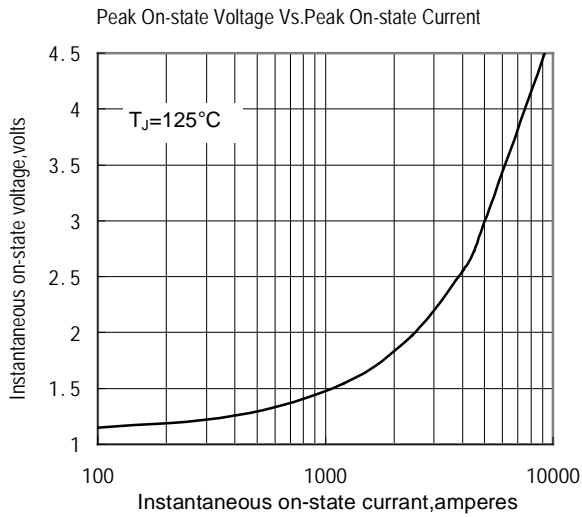


Fig.1

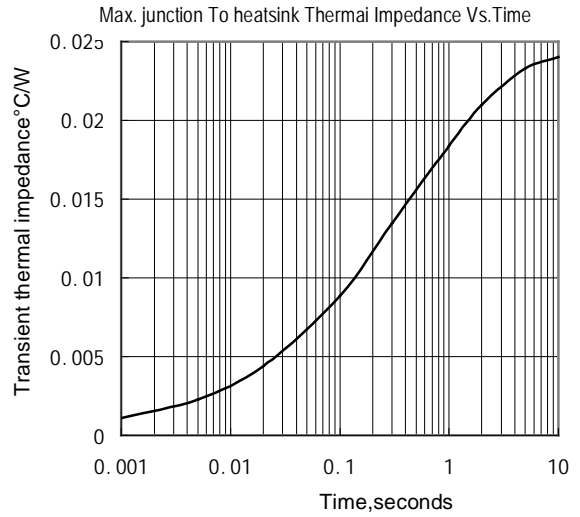


Fig.2

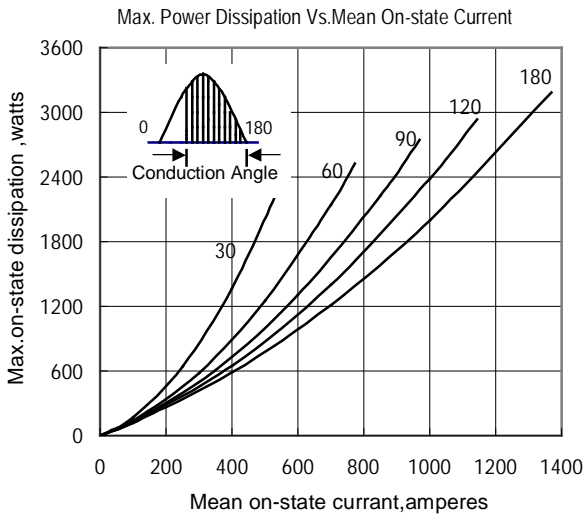


Fig.3

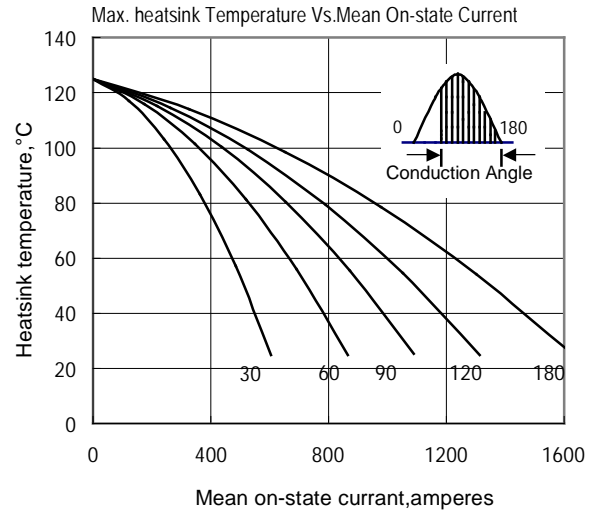


Fig.4

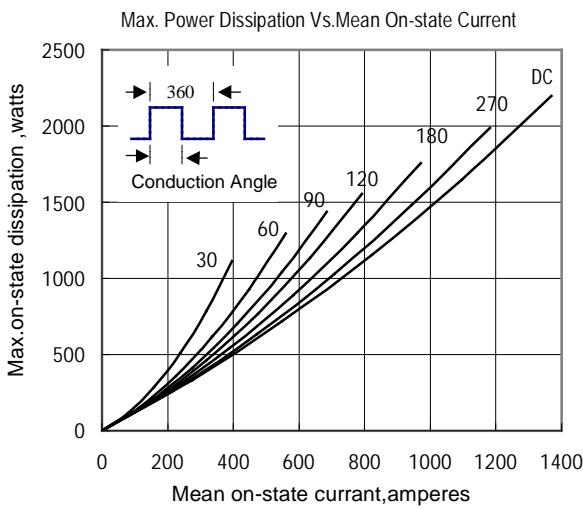


Fig.5

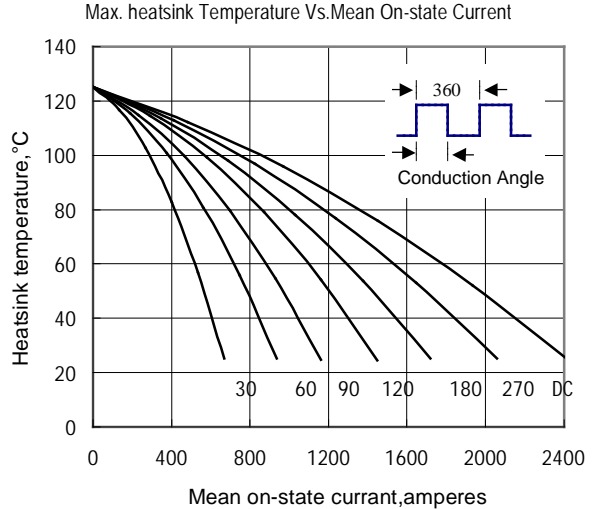


Fig.6

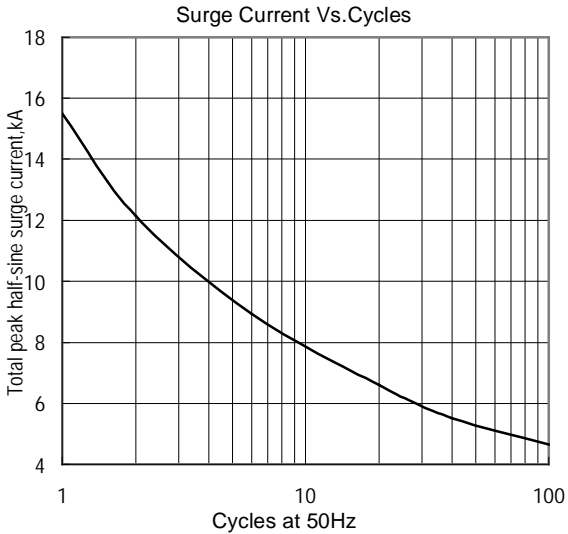


Fig.7

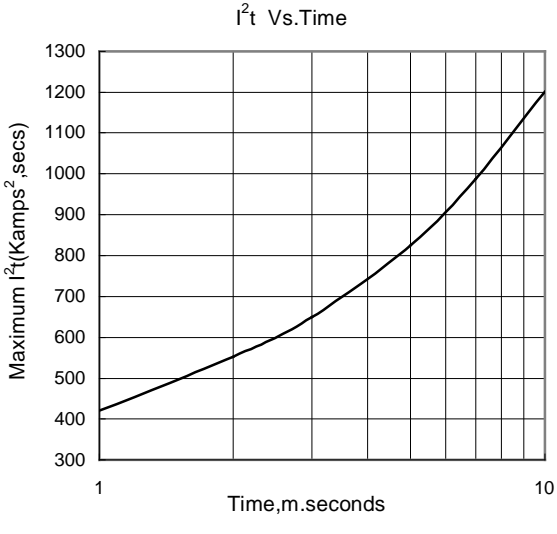


Fig.8

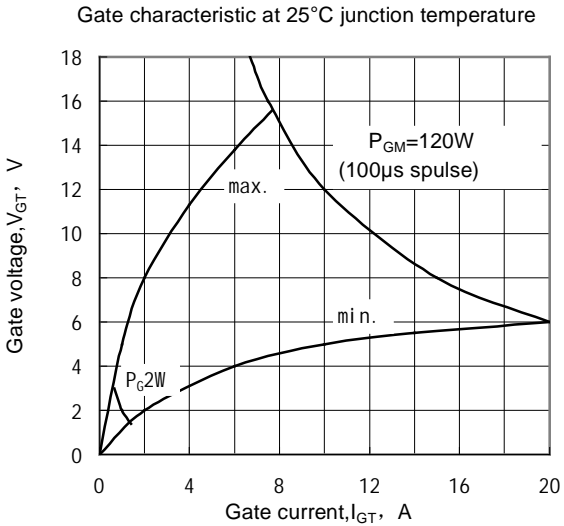


Fig.9

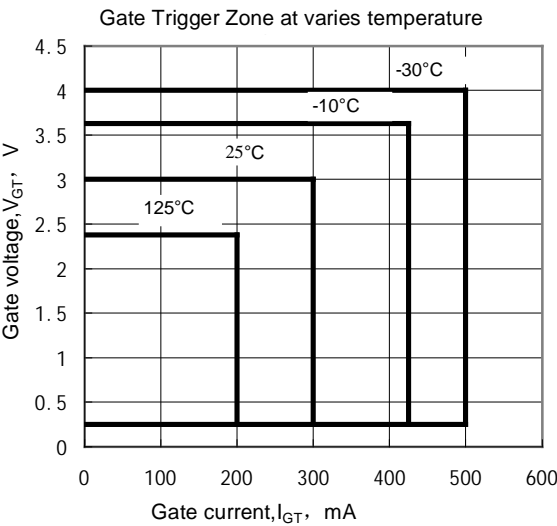


Fig.10

Outline:

