Y76KPM

PHASE CONTROL THYRISTOR

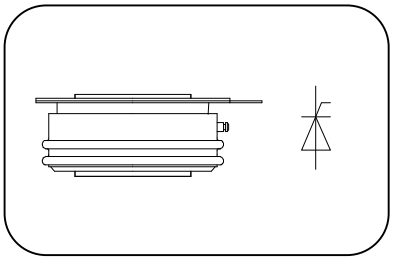
Features:

- **n** Center amplifying gate
- **n** Metal case with ceramic insulator
- **n** Low on-state and switching losses

Typical Applications

- **n** AC controllers
- **n** DC and AC motor control
- **n** Controlled rectifiers

$I_{T(AV)}$	2049 A
V_{DRM}/V_{RRM}	4300-5500V
I_{TSM}	24.6 KA
I^2t	3026 10^3A^2S



SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Double side cooled, T_{hs}=55°C	125			2049	A
V_{DRM} V_{RRM}	Repetitive peak off-state voltage Repetitive peak reverse voltage	V_{DRM}&V_{RRM} tp=10ms V_{DSM}&V_{RSM}= V_{DRM}&V_{RRM}+100V	125	4300		5500	V
I_{DRM} I_{RRM}	Repetitive peak current	V_{DM}= V_{DRM} V_{RM}= V_{RRM}	125			120	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=0.6V_{RRM}	125			24.6	KA
I^2t	I^2T for fusing coordination					3026	A^2s*10^3
V_{TO}	Threshold voltage		125			1.30	V
r_T	On-state slop resistance					0.42	mW
V_{TM}	Peak on-state voltage	I_{TM}=3000A, F=41KN	125			2.56	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=0.67V_{DRM}	125			800	V/μs
di/dt	Critical rate of rise of on-state current	V_{DM}= 67%V_{DRM} to 4000A, Gate pulse t_r ≤0.5 μ s I_{GM}=1.5A Repetitive	125			250	A/μs
I_{rm}	Reverse recovery current	I_{TM}=2000A,tp=1000μs, di/dt=-20A/μs, V_R=50V	125			250	A
t_{rr}	Reverse recovery time					24	μs
Q_{rr}	Recovery charge					3000	μC
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	40		300	mA
V_{GT}	Gate trigger voltage			0.8		3.0	V
I_H	Holding current			20		250	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.3			V
$R_{th(j-h)}$	Thermal resistance Junction to heat sink	At 180^0 sine, double side cooled Clamping force 40.0KN				0.01	°C /W
F_m	Mounting force			35		47	KN
T_{stg}	Stored temperature			-40		140	°C
W_t	Weight				1100		g
Outline	KT73cT						

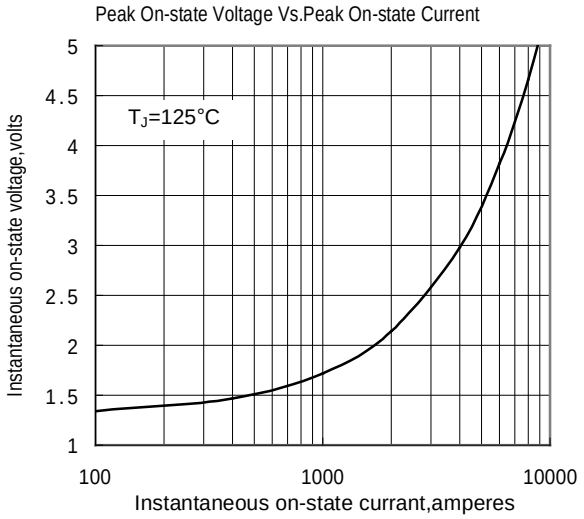


Fig.1

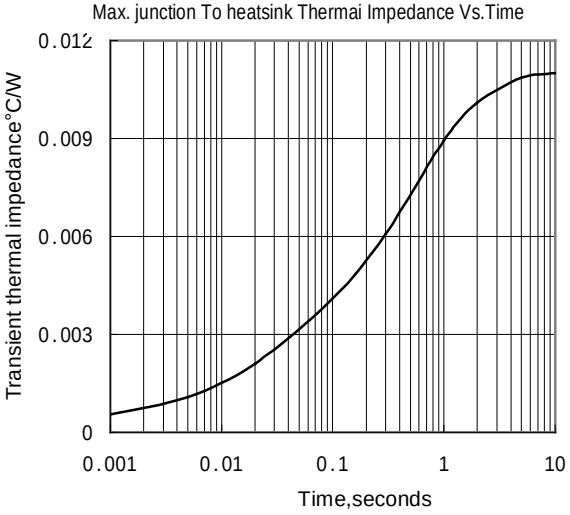


Fig.2

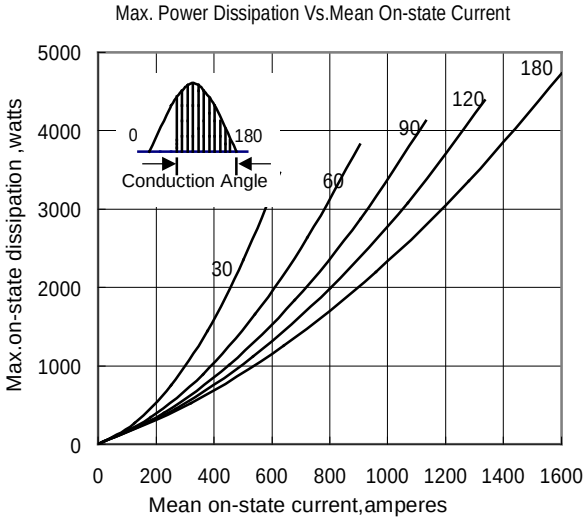


Fig.3

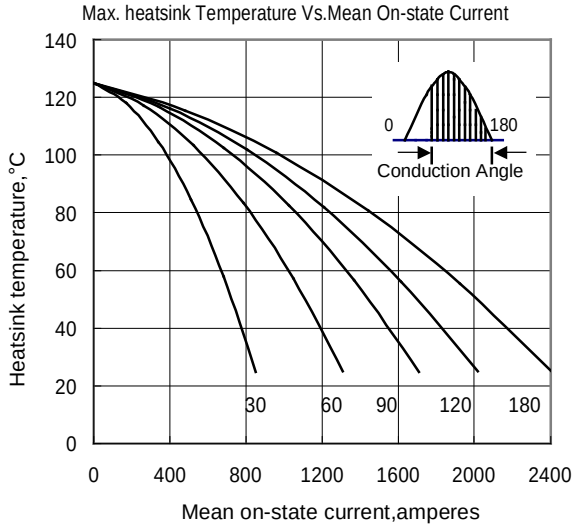


Fig.4

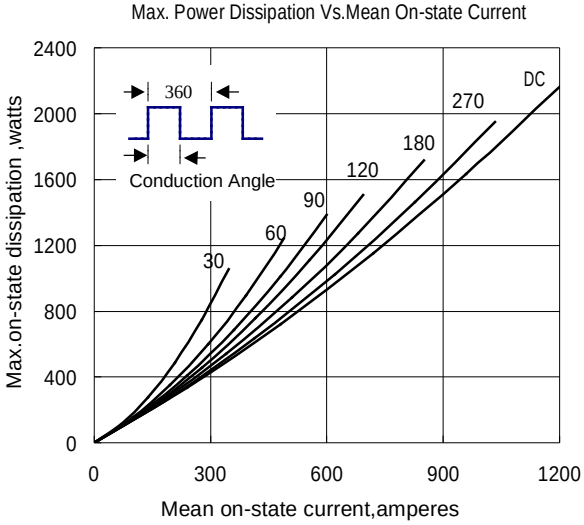


Fig.5

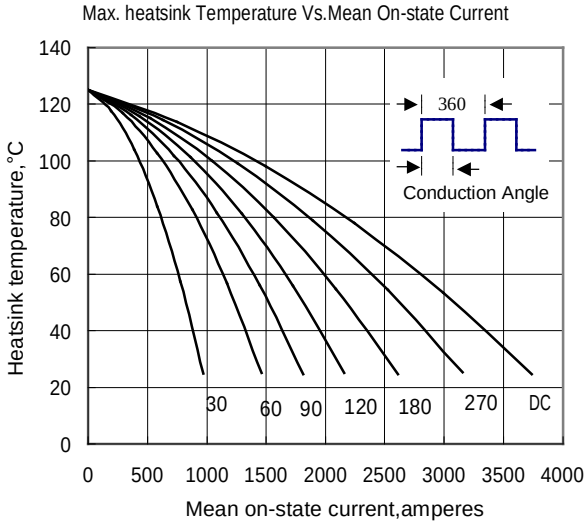


Fig.6

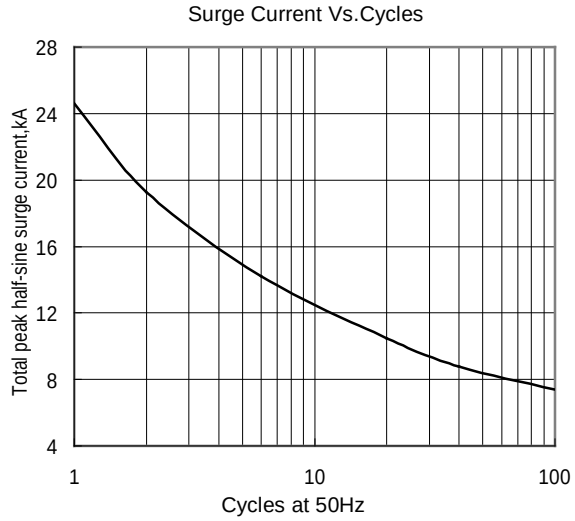


Fig.7

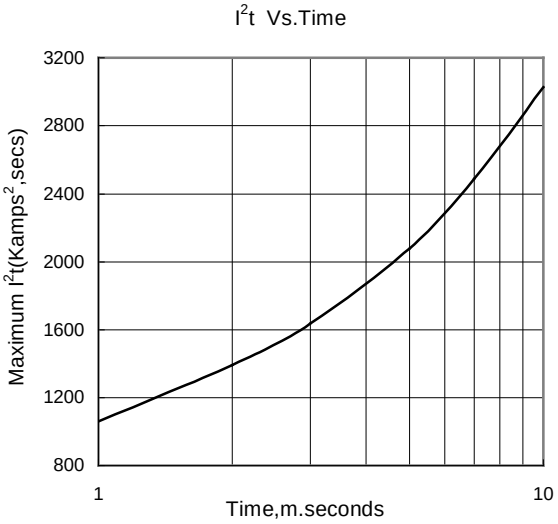


Fig.8

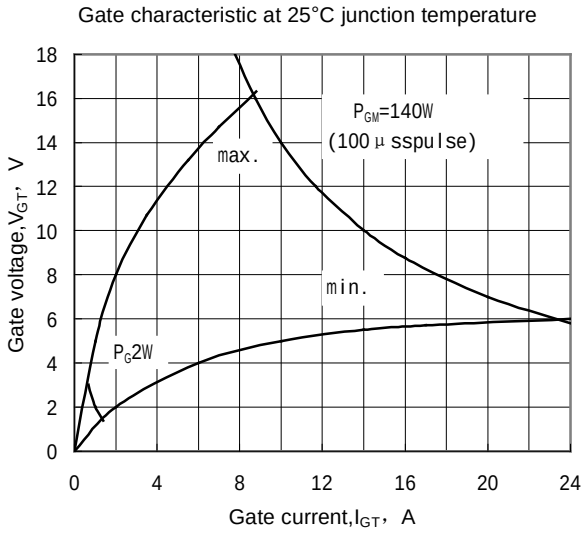


Fig.9

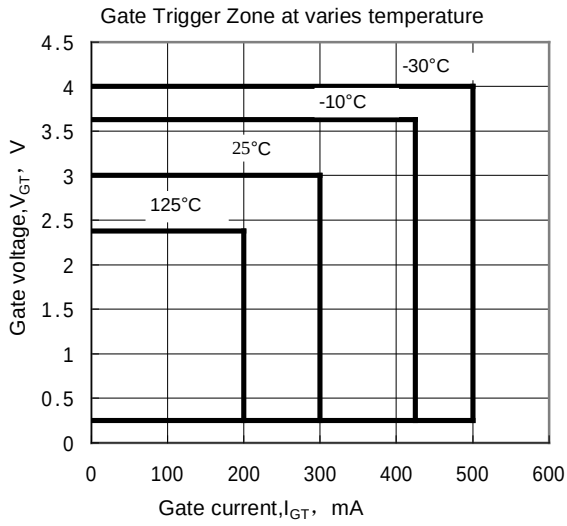


Fig.10

Outline: